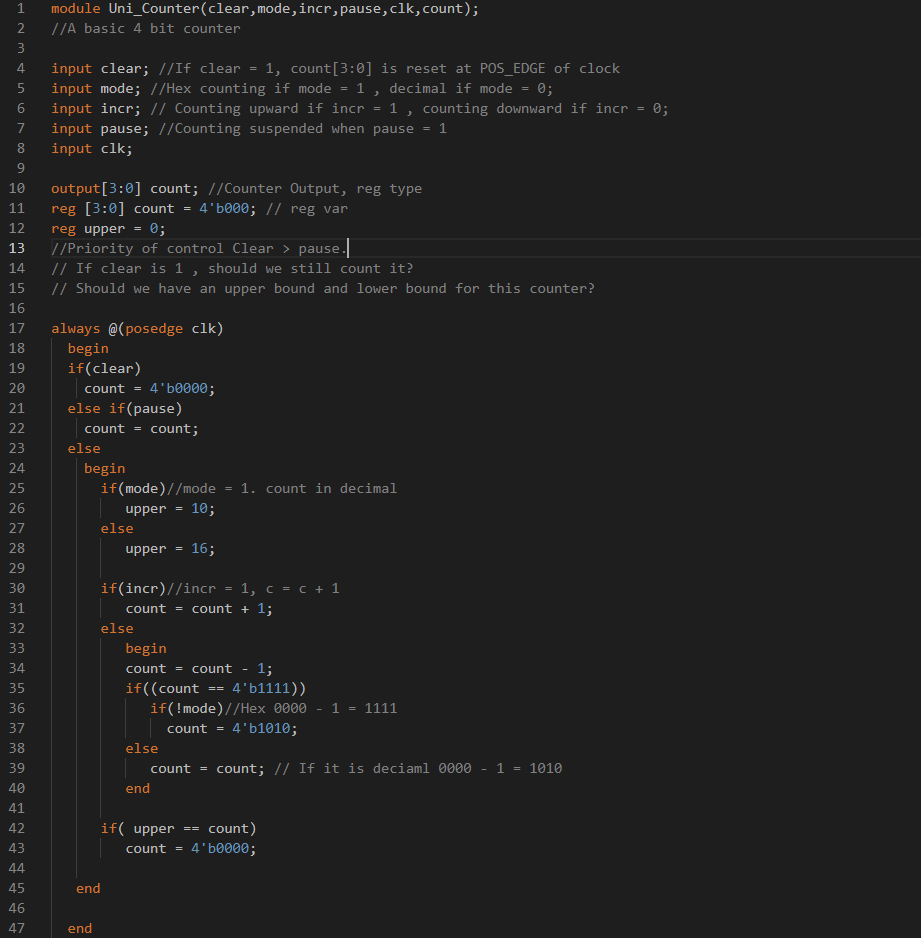
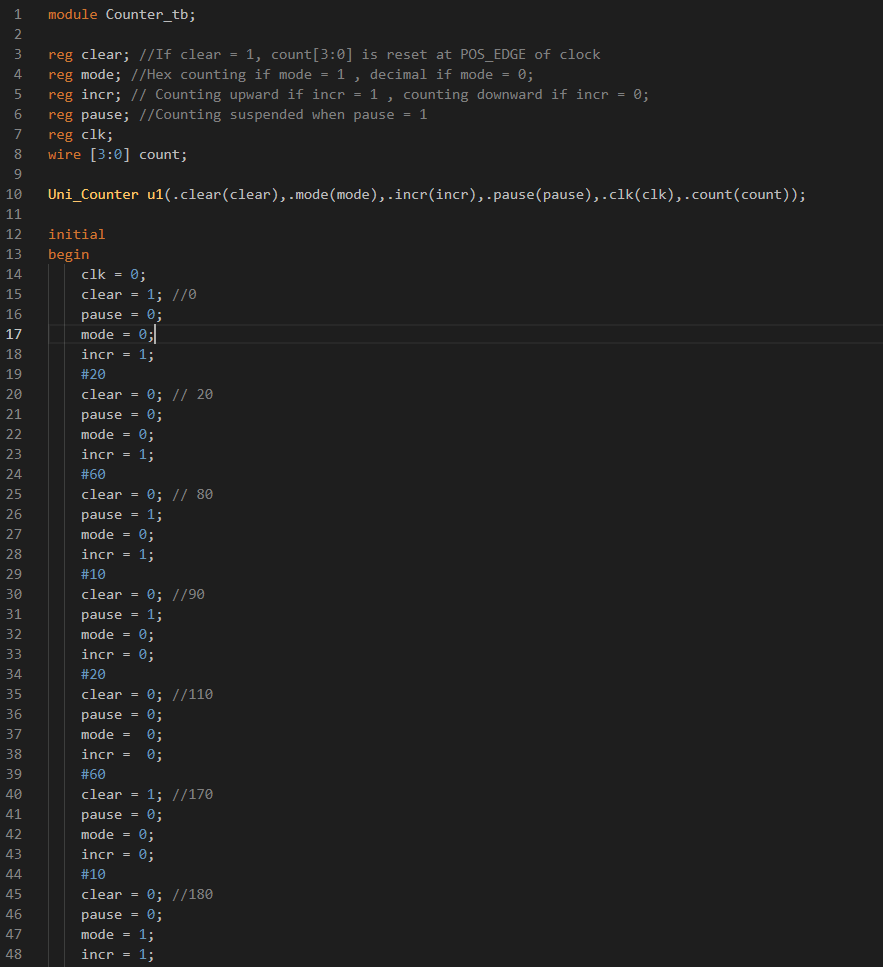
HDL HW3 report

Q1 Universal 4 bit counter

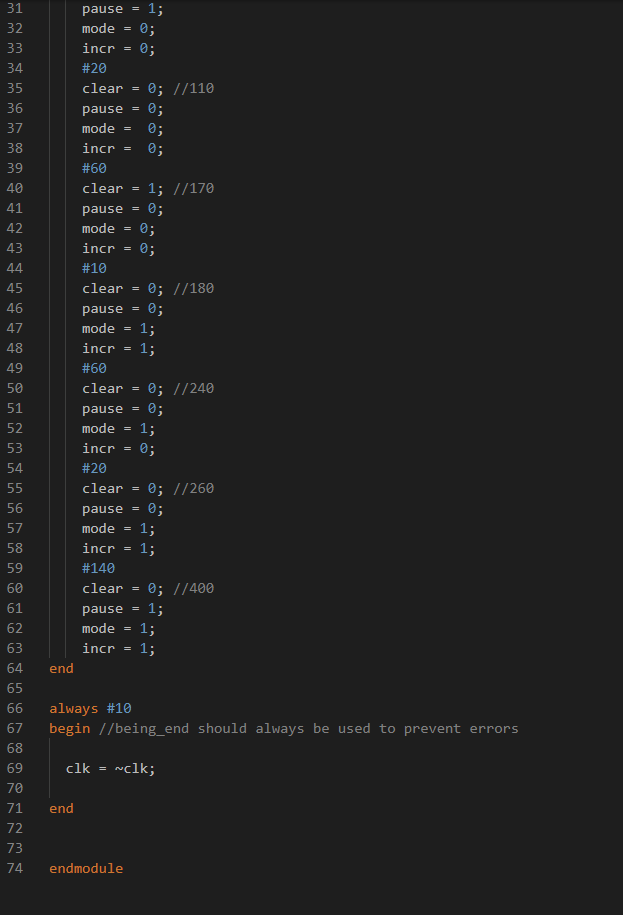
Code for universal counter.



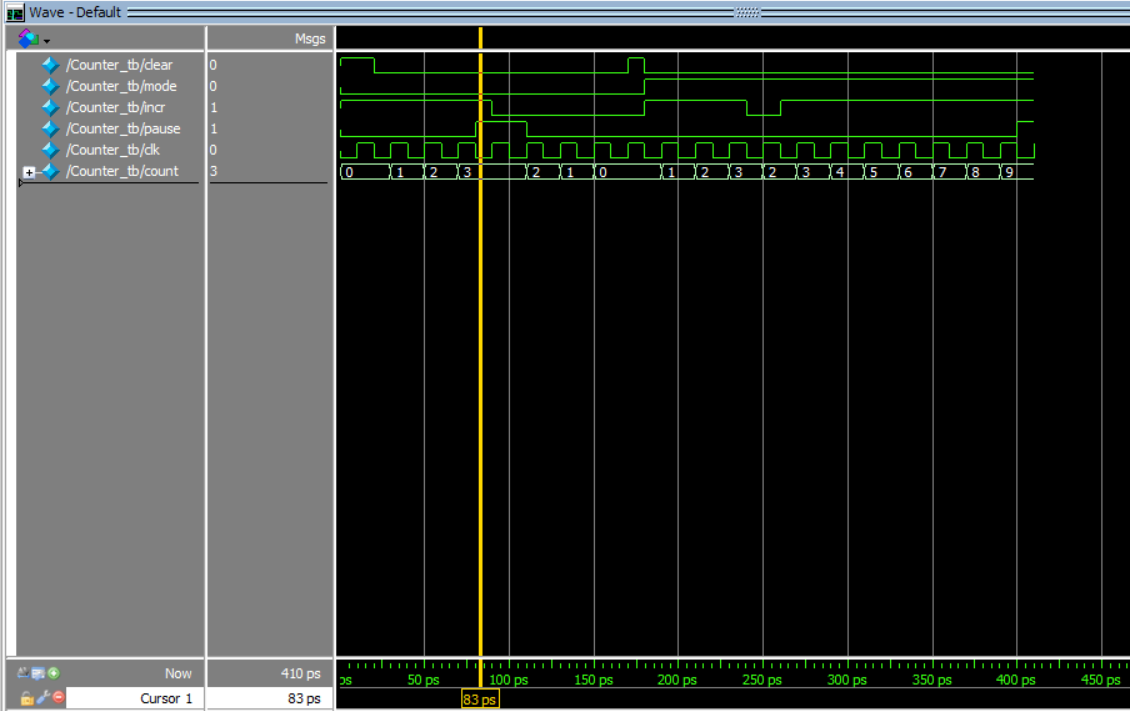
Testbench for universal counter



TestBench part2



The waveform for universal counter



@t=0 mode:0 incr:1 pause:1 clk:0 Counter Paused

@t=90 clear:1 mode:0 incr:1 pause:0 clk:0 decrementing

@t=171 clear:1 mode:0 incr:0 pause:0 clk:0 Value get reseted to 0

@t=190 clear:0 mode:1 incr:1 pause:0 clk:1 Incrementing

@t=241 clear:0 mode:1 incr:0 pause:0 clk:0 Decrementing

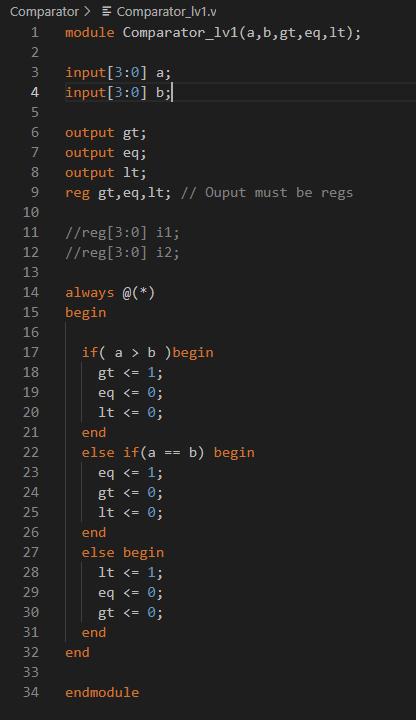
@t=261 clear:0 mode:1 incr:1 pause:0 clk:1 Adding up mode decimal.

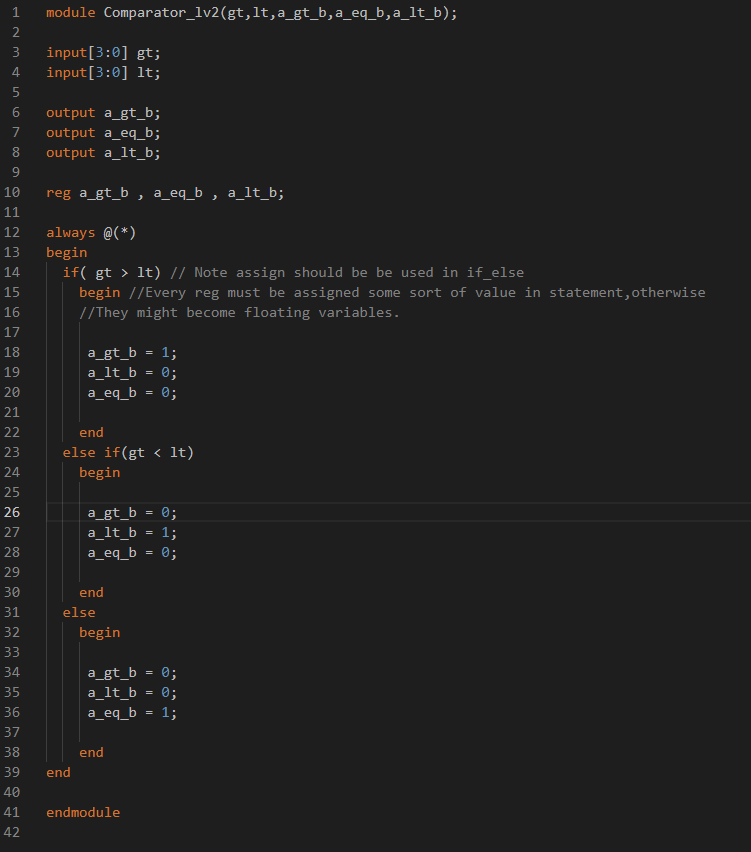
Actually this tesetbench cannot test out the which mode we are running

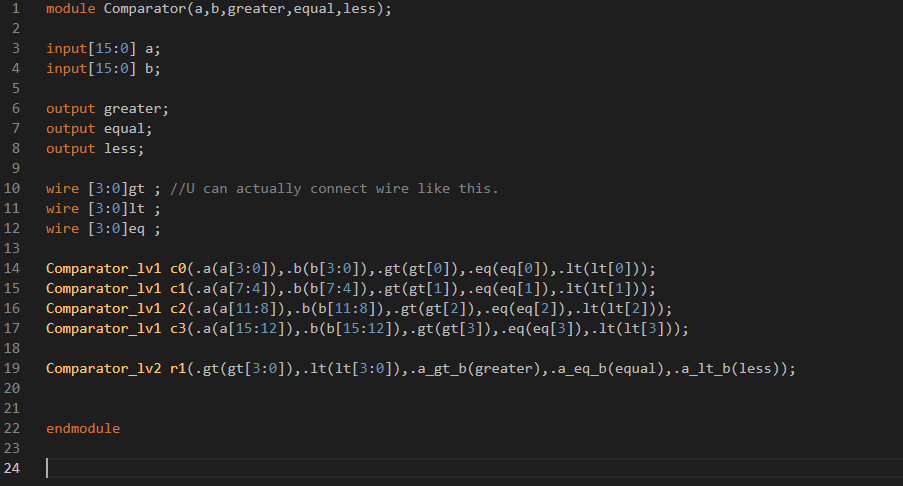
i.e. whether it is mode Hex or mode decimal is right or not but anyways~

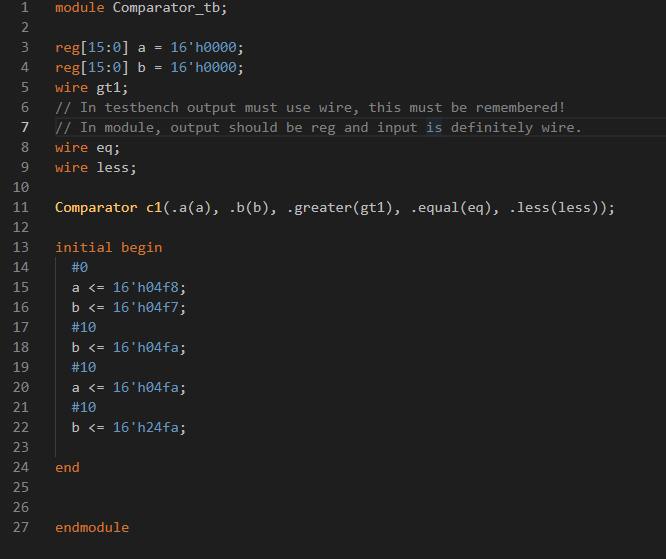
Q2 Comparator:

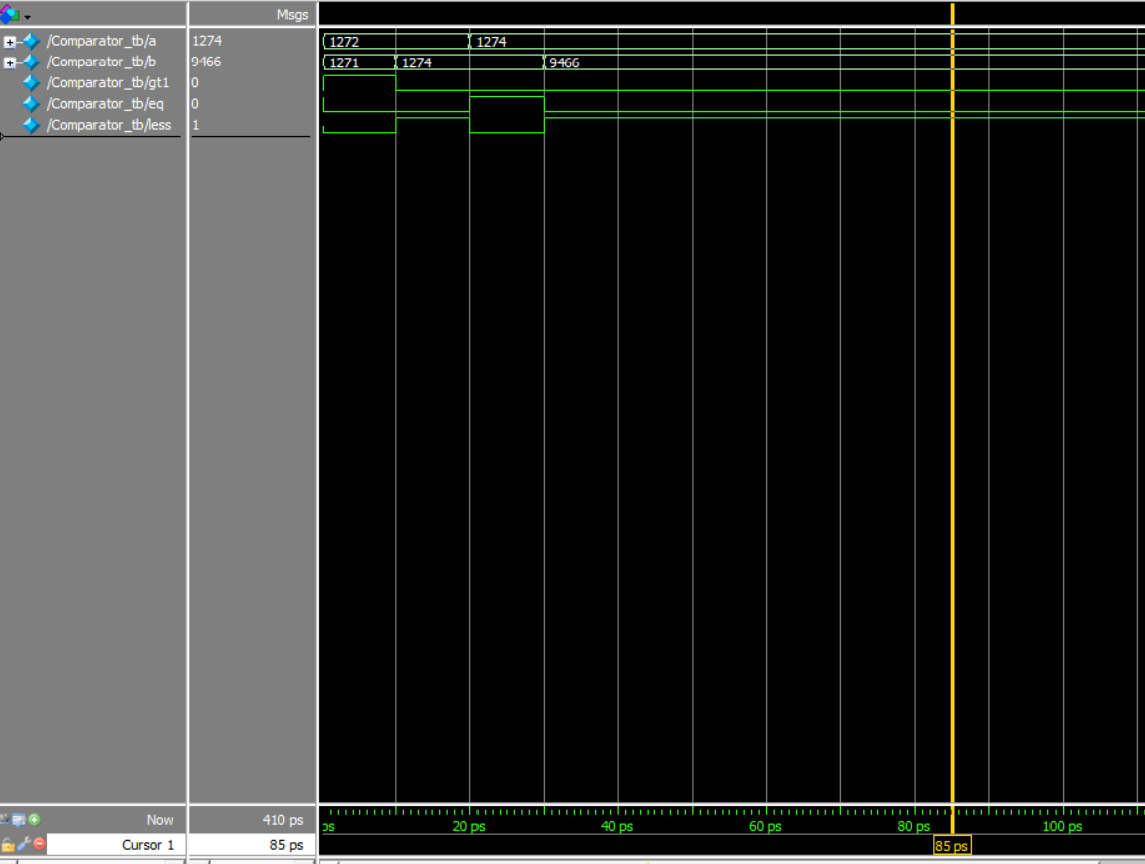
Code for Level 1 Comparator x4



Code for Lv2 Comparator x1

Code for testbench and comparator main.



Comparator wave form, one with delay one without

1. 1272 > 1271 thus gt1 = 1 eq = 0 less = 0
2. 1272 < 1274 gt1 = 0 eq = 0 less = 1
3. 1274 = 1274 gt1 = 0 eq = 1 less = 0
4. 1274 < 9466 gt1 = 0 eq = 0 less = 1

Waveform with Delay. Due to the existence of delay, the value of gt1 eq and less would be floating value due to the propagation delay. And since eq#5 > bgt#3 and less#4, thus the critical path for this 2 level comparator is from gt #3 + eq #5 it is 8. Since the first stage eq would simply be discarded.

